Electronic Version

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Description

PARASITIC CAPACITANCE-PREVENTING DUMMY SOLDER BUMP STRUCTURE AND METHOD OF MAKING THE SAME

BACKGROUND OF INVENTION

[0001] 1.Field of the Invention

[0002] The present invention relates to a method of forming a solder bump structure, and more specifically, to a method of forming a parasitic capacitance-preventing dummy solder bump structure.

[0003] 2.Description of the Prior Art

[0004] High performance microelectronic devices often use solder balls or solder bumps for electrically and mechanically interconnection to other microelectronic devices. For instance, a very large scale integration (VLSI) chip may be electrically connected to a circuit board or other next level packaging substrate by using solder balls or solder bumps. This connection technology is also referred to as

"Controlled Collapse Chip Connection (C4)" or "flip chip" technology. The flip chip technology is an area array connection technology and includes reflowing a body of solder onto a bond pad to form a solder bump, so as to electrically connect an IC die to a packaging board.

[0005] Please refer to Fig.1 to Fig.4 of schematic views of forming a solder bump according to the prior art. As shown in Fig.1, a surface of a substrate 10 comprises a first area 12 and a second area 14, and at least one conductive layer 16 is positioned on the surface of the substrate 10. Normally, the substrate 10 is a semiconductor wafer with circuits formed inside the semiconductor wafer, and the first area 12 and the second area 14 are respectively a central area and a border area of the surface of the substrate 10.

[0006] As shown in Fig.2, a chemical vapor deposition (CVD) process is performed to form a dielectric layer 18 on the substrate 10 to cover the conductive layer 16. An etching process is then performed to form at least one via hole 20 in portions of the dielectric layer 18 within the first area 12 down to a surface of the conductive layer 16. By performing a deposition process, a via plug 22, comprising tungsten, is formed in each via hole 20. A chemical mechanical polishing (CMP) process is performed thereafter

to make a top surface of the via plug 22 approximately aligned with a top surface of the dielectric layer 18.

[0007] As shown in Fig.3, a metal pad 24, comprising either copper or aluminum, is formed within each of a plurality of predetermined regions within the first area 12 and the second area 14. A CVD process and an etching process are then performed to form a passivation layer 26 on portions of the dielectric layer 18 not covered by the metal pad 24. As shown in Fig.4, an under bump metallurgy (UBM) layer 28 is formed on each metal pad 24 by performing a sputtering process and an etching process. Finally, a solder bump 30 is formed on each UBM layer 28. Wherein portions of the solder bumps 30 formed within the second area are employ as dummy solder bumps to make the layout of the solder bumps 30 on the surface of the substrate 10 symmetrical, so as to improve the fluidity of an underfill liquid compound in subsequent packaging processes.

[0008] However, as technology progresses, the process line width of semiconductor manufacturing decreases as well. Parasitic capacitance therefore occurs between the metal pad 24 and the conductive layer 16 due to the shortened distance between the metal pad 24 and the conductive layer

as the thickness of the dielectric layer 18 is narrowed, leading to the defective electrical performance or even circuit fail of the device.

SUMMARY OF INVENTION

[0009] It is therefore a primary object of the present invention to provide a method of the forming a parasitic capacitance-preventing dummy solder bump structure so as to assure the electrical performance of a semiconductor device.

[0010] According to the claimed invention, a surface of a substrate comprises a first area and a second area, and at least one conductive layer is formed on the surface of the substrate. At the beginning of the method, a chemical vapor deposition (CVD) process is performed to form a dielectric layer on the substrate to cover the conductive layer. At least one via plug is then formed in portions of the dielectric layer within the first area down to a surface of the conductive layer. At least one metal pad electrically connected to the via plug is formed thereafter. By performing an UBM process, at least one UBM layer is formed to cover both the metal pad within the first area and portions of the dielectric layer within the second area. Finally, a solder bump is formed on the UBM layer. Wherein the solder bump formed within the second area is employed

as a dummy solder bump to improve the fluidity of an underfill liquid compound in subsequent packaging processes.

[0011] It is an advantage of the present invention against the prior art that the dummy solder bump in the present invention is formed on the UBM layer positioned on the dielectric layer, so that the metal pad between the UBM layer and the dielectric layer according to the prior art is neglected. The parasitic capacitance occurred between the metal pad under the dummy solder bump and the neighboring metal wire as described in the prior art is prevented. Consequently, the fluidity of an underfill liquid compound in subsequent packaging processes is significantly improved without reducing the electrical performance of the device, and the manufacturing yield rate is increased as well.

[0012] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the multiple figures and drawings.

Brief Description of Drawings

[0013] Fig.1 to Fig.4 are schematic views of forming a solder

bump according to the prior art.

[0014] Fig.5 to Fig.9 are schematic views of forming a parasitic capacitance-preventing dummy solder bump structure according to the present invention.

DETAILED DESCRIPTION

[0015] Please refer to Fig.5 to Fig.9 of schematic views of forming a parasitic capacitance-preventing dummy solder bump structure according to the present invention. As shown in Fig.5, a substrate 40 comprises at least patterned conductive layer 46 positioned on a surface of the substrate 40. The surface of the substrate 40 comprises a first area 42 and a second area 44. Normally, the substrate 40 is a semiconductor wafer with circuits formed inside the semiconductor wafer, and the first area 42 and the second area 44 are respectively a central area and a border area of the surface of the substrate 40.

[0016] As shown in Fig.6, a chemical vapor deposition (CVD) process is performed to form a dielectric layer 48, comprising either silicon nitride or silicon oxide, on the substrate 40 to cover the conductive layer 46. A passivation layer 50, comprising either silicon nitride or silicon oxide, is formed thereafter on the dielectric layer 48. Alternatively, in another embodiment of the present invention, the dielectric

layer 48, comprising either silicon nitride or silicon oxide, is formed to cover the conductive layer 48 without the passivation layer 50 subsequently formed on the dielectric layer.

[0017] As shown in Fig.7, an etching process is performed to form at least one via hole 52 in portions of the dielectric layer 48 within the first area 42 down to a top surface of the conductive layer 48. A via plug 54 is then formed to fill each via hole 52 by performing a deposition process. Normally, the via plug 54 comprises either one of titanium (Ti), titanium nitride (TiN), tungsten (W), aluminum (Al), copper (Cu) or copper-aluminum alloy (Cu-Al alloy), and is alternatively formed by a sputtering process.

[0018] As shown in Fig.8, at least one metal pad 56 electrically connected to the via plug 54 is formed, and a sputtering process and an etching process are performed to form at least one under bump metallurgy layer (UBM layer) 58 to cover both the metal pad 56 within the first area 42 and portions of the passivation layer 50 within the second area 44.

[0019] Finally, as shown in Fig.9, a solder bump 60 is formed on each UBM layer 58 at the end of the method. Wherein the solder bump 60 formed within the second area 44 is em-

ployed as a dummy solder bump to make the layout of the surface of the substrate 40 symmetrical, so as to improve the fluidity of an underfill liquid compound in subsequent packaging processes.

[0020] It is emphasized that the metal pad 56 formed on the via plug 54 is employed to reinforce the adhesion between the UBM layer 58 and the via plug 54, so that no metal pad 56 is formed within the second area 44. In another embodiment of the present invention, the metal pad 56, under either the solder bump 60 within the first area 42 or the dummy solder bump 60 within the second area 44, is neglected.

[0021] In comparison with the prior, the present invention reveal a method of forming the solder bump 60 on the UBM layer 58 after performing a sputtering process to form the UBM layer 58 on either the metal pad 56 within the first area 42 or the passivation layer 50 within the second area 44, so as to use the solder bump 60 within the second area 44 as a dummy solder bump to make the layout of the surface of the substrate 40 symmetrical. Therefore, the fluidity of an underfill liquid compound in subsequent packaging processes is significantly improved. As the thickness of the dielectric layer 48 decreases due to the

narrowed process line width, the parasitic capacitance occurred between the metal pad under the dummy solder bump and the neighboring metal wires as described in the prior art is prevented. Consequently, the fluidity of an underfill liquid compound in subsequent packaging processes is improved without reducing the electrical performance of the device.

[0022] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bound of the appended claims.